ABSTRACT

A method and processor for interrupt processing operate to save processor cycles during the handling of interrupts. More particularly, upon an interrupt, the first instruction from an interrupt service routine (ISR) is loaded into an instruction register for immediate execution to save at least one cycle of interrupt instruction fetching. Simultaneously, the address of the second instruction from the ISR is stored into a program counter. Also, the next instruction in the regular program cycle for execution is taken from a prefetch register and stored in a holding register (or to the stack). Subsequently, the second instruction from the ISR is fetched and executed and the interrupt is serviced. When finished, the next regular instruction for execution is loaded into the prefetch register from the holding register (or stack) for subsequent execution. The program counter and a status register are restored from the stack. In the next cycle, the instruction from the holding register is executed and the following instruction is fetched into the prefetch. These steps save at least one cycle in processing interrupts.